WHAT IS CLAIMED IS:

1. A phase blending circuit for generating a plurality of signals differing in phase relative to an early phase signal, comprising:

a current source having a common output node;

one or more delay elements; and

one or more switches to selectively couple one or more of the delay elements to the common output node of the current source, wherein a time required for a voltage level at the common output node to fall below a threshold level after assertion of the early phase signal is dependent on which of the one or more delay elements are coupled to the common output node.

2. The phase blending circuit of claim 1, wherein the one or more delay elements comprises at least one transistor to provide a path for current flow from the common output node of the current source in response to assertion of the early phase signal.

3. The phase blending circuit of claim 2, wherein the at least one transistor comprises a plurality of transistors having different dimensions.

4. The phase blending circuit of claim 3, wherein the dimensions of the transistors are selected such that the phases of the plurality of signals are separated by a substantially equal phase.

5. The phase blending circuit of claim 1, wherein the one or more delay elements comprises at least one capacitor coupled with the common output node of the current source.

6. The phase blending circuit of claim 5, wherein the at least one capacitor comprises a plurality of capacitors having different values of capacitance.

7. The phase blending circuit of claim 6, wherein the capacitor values are selected such that the phases of the plurality of signals are separated by a substantially equal phase.

8. A phase blending circuit for generating a plurality of signals differing in phase relative to an early phase signal, comprising:

a current source having a common output node and a control input for disabling the current source when a late phase signal trailing the early phase signal is asserted;

a comparator having an input coupled with the common output node of the current source;

a plurality of delay elements;

a path for current flow from the common output node when the early phase signal is asserted; and

a plurality of switches to selectively couple one or more of the delay elements to the output node of the current source for varying the time required for a voltage level of the common output node to fall below a threshold level as a result of current flow through the path.

9. The phase blending circuit of claim 8, wherein the path for current flow comprises at least one transistor receiving the early phase signal as an input.

10. The phase blending circuit of claim 9, wherein the at least one transistor is one of the delay elements coupled to the common output node of the current source via one of the switches.

11. The phase blending circuit of claim 9, wherein the at least one transistor comprises an NMOS transistor and the current source comprises a PMOS transistor.

12. The phase blending circuit of claim 9, wherein the path for current flow further comprises at least one transistor receiving the late phase signal as an input.

13. The phase blending circuit of claim 8, wherein the one or more delay elements are configured to allow generation of a plurality of signals having phases separated by a substantially equal phase.

14. A delay locked loop circuit for generating an output signal aligned with an input signal, comprising:

a delay line for providing phase signals delayed relative to the input signal by one or more of unit delays;

a phase blending circuit for generating a blended phase signal having a phase between early and late phase signals provided by the delay line, the phase blending circuit comprising a current source and one or more delay elements for selectively coupling to a common output node of the current source, wherein a time required for a voltage level at the common output node to fall below a threshold level after assertion of the early phase signal is dependent on which of the one or more delay elements are coupled to the common output node; and

control logic configured to monitor skew between the input and output signals and, based on the skew, generate one or more control signals to select the early and late signals provided to the phase blending circuit and to selectively couple one or more of the delay elements to the common output node.

15. The delay locked loop circuit of claim 14, wherein the control logic is further configured to:

(a) determine if the input and output signals are aligned within an accepted tolerance;

(b) if not, modify the one or more control signals to couple a different one or more of the delay elements to the common output node; and

(c) repeat steps (a)-(b) until the input and output signals are aligned within the accepted tolerance.

16. The delay locked loop circuit of claim 14, wherein:

the phase blending circuit further comprises a comparator having an input node coupled with the common output node of the current source; and

the threshold level is the threshold level of the comparator.

17. The delay locked loop circuit of claim 16, wherein the output signal is generated on an output node of the comparator.

18. A dynamic random access memory (DRAM) device, comprising:

one or more memory elements; and

a delay locked loop circuit for synchronizing data output from the one or more memory elements with a clock signal comprising (i) a delay line, (ii) a phase blending circuit comprising a current source and one or more delay elements for selectively coupling to a common output node of the current source, wherein a time required for a voltage level at the common output node to fall below a threshold level after assertion of an early phase signal provided by the delay line is dependent on which of the one or more delay elements are coupled to the common output node, and (iii) control logic configured to monitor skew between the input and output signals and, based on the skew, generate one or more control signals to select the early signal provided to the phase blending circuit by the delay line and to selectively couple one or more of the delay elements to the common output node.

19. The DRAM device of claim 18, wherein the one or more delay elements comprise a plurality of transistors having different dimensions.

20. The DRAM device of claim 18, wherein the one or more delay elements comprise a plurality of capacitors.

21. The DRAM device of claim 20, wherein the plurality of capacitors are of the same type as capacitors utilized in the memory elements.

22. A method for generating a phase signal having a phase intermediate to phases of an early signal and a late signal, comprising:

coupling the early signal to a control input of one or more switches to provide a path for current flow from a common output node of a current source through the one or more switches when the early signal is asserted; and

closing one or more switches to selectively couple one or more delay elements to the common output node of the current source, wherein a time required for a voltage level of the common output node to fall below a threshold level as a result of the current flow is dependent on which of the one or more switches are closed.

23. The method of claim 22, further comprising coupling the late signal to a control input of the current source to disable the current source when the late signal is asserted.

24. The method of claim 22, wherein the one or more delay elements comprise one or more transistors.

25. The method of claim 24, wherein the one or more switches comprise the one or more transistors.

26. The method of claim 22, wherein the one or more delay elements comprise one or more capacitors.

27. The method of claim 22, wherein:

the late signal trails the early signal by a unit delay; and

the switches and delay elements are configured to provide the delayed signal differing in phase from the early signal by a fraction of the unit delay, wherein the fraction depends on which of the switches are closed.